Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **V OUT**
2. **V IN**
3. **GND**

**.047”**

**.039”**

**3**

**1 2**

**5**

**TR**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .039” X .047” DATE: 8/17/21**

**MFG: SILICON SUPPLIES THICKNESS .011” P/N: 78L05**

**DG 10.1.2**

#### Rev B, 7/1